Imperial College
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# Lecture 3

# Understanding op-amp specifications

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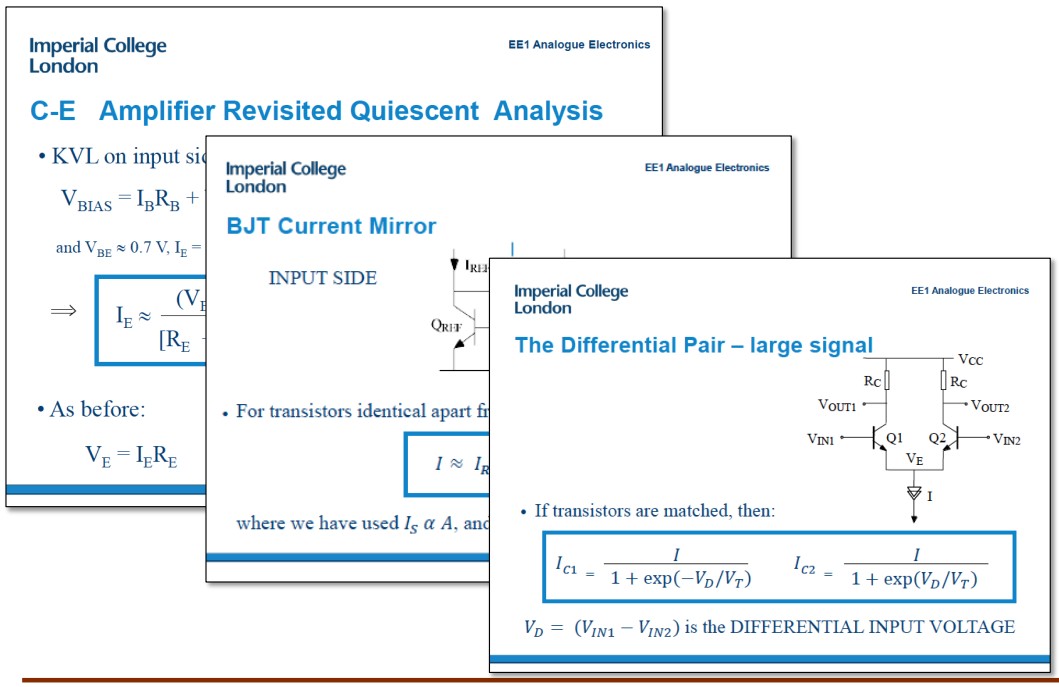
In this week's lecture, I will examine the high-level architecture of an op-amp. The purpose of this is to explain where the characteristics of a typical modern op-amp come from.

In Year 1, you have already learned how different types of transistor circuits work: common-emitter amplifier, differential amplifier, emitter follower etc.. You have also used SPICE to simulate, at transistor level, a typical operational amplifier as part of the Laboratory coursework.

In this lecture, we will examine the difference between BJT and MOSFET op-amps. In particular, we will examine the architecture of the output stage of the op-amp.

Finally, you will learn how to interpret the key specification of an op-amp from the datasheet.

# What you should know already?



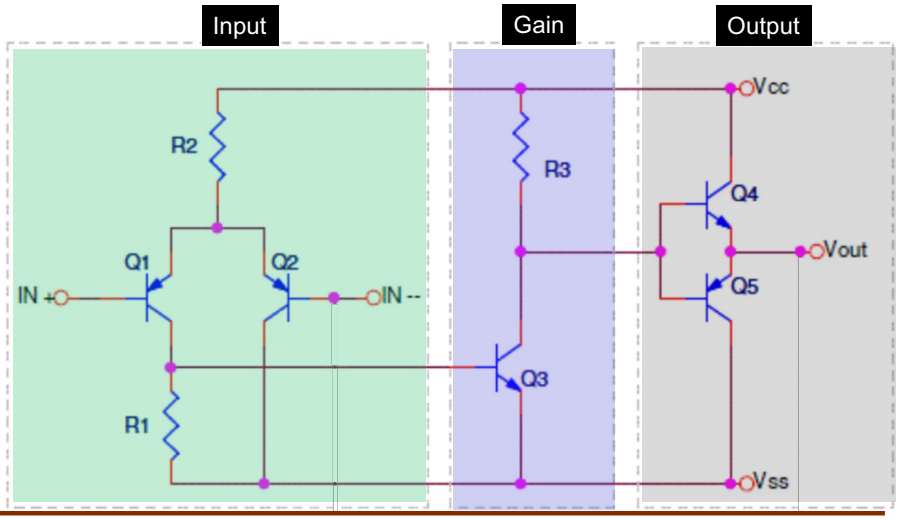

Here are extracts of some of the slices you used in the Analysis and Design of Circuits (ADC) module in Year 1, where you have learned all the equations relating to currents and voltages in different configurations of bipolar transistor circuits.

While knowing equations governing the working of circuits is important, and the ability to analyse circuits in a rigorous manner is essential for an electronic engineer, it is also important for you acquire some intuition about circuits. Such intuitions will allow you to develop deeper insights on why you might consider adding a transistor at a certain place may be worth exploring. This ability would allow you to "see" how a circuit works and understand why it has limitations. This hopeful leads you inventing new circuits that work better than previous designs.

The approach taken in this lecture is therefore NOT about designing at transistor level, but acquire a high-level understanding on the characteristics of op-amps and why they behave the way they do.

## Inside a typical BJT op-amp

- Three stages architecture:
  1. **Differential input stage** – long-tail pair (Yr 1 Circuits part 2, adc_9, slides 8-14)
  2. **Voltage gain stage** – common emitter amp (adc_6, slides 3-7)
  3. **Output drive stage** – push-pull circuit






Let us now turn our attention to a generic bipolar junction transistor op-amp architecture. These were popular in the early era of analogue integrated amplifiers. Most notably are the LM741 and LM301 op-amps, and the LM386 audio amplifier that was used in our lab experiments in the past. These designs were very popular forty years ago!

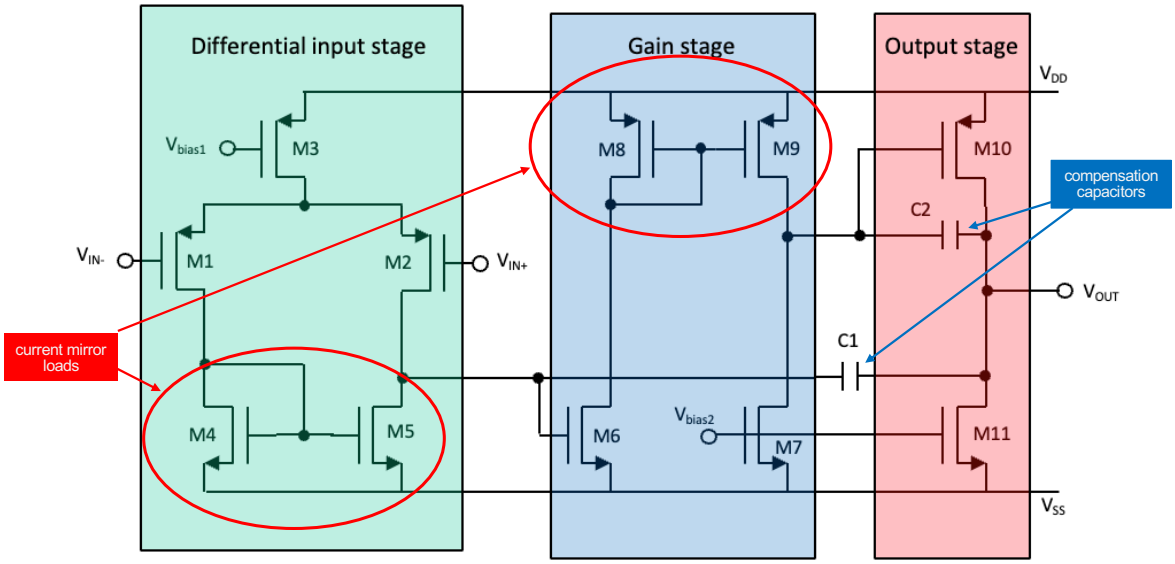
You have already encountered this in Year 1 Spring Term Lab ADC_4, when you simulated an op-amp at transistor level using SPICE.

A typical op-amp consists of three stages:

1) The input stage provides **differential inputs** IN+ and IN- and gives the op-amp the ability to reject common-mode signals. (Common-mode signal is a signal that is applied to both IN+ and IN- simultaneously.)
2) The second stage is a common-emitter gain stage **that provides most of the gain** in an op-amp.
3) The third stage is the **output stage** that provides the output current capability.

## Inside a typical MOSFET op-amp

- Early MOSFET op-amp follows similar architecture to the BJT version.






Most modern op-amps are now based on MOSFET transistor. Here is an overview of an early MOSFET op-amp architecture, which also has three main stages as in the previous slide.

- M1, M2 (p-type) provide the differential stage that amplifies the difference in $V_{IN+}$ and $V_{IN-}$.
- M3 generates the tails current as before. When $V_{IN+} = V_{IN-}$, the current through M1 and M2 are identical because the two transistors have the same $V_{GS}$.
- Unlike the BJT case, the load of the differential circuit is not resistive but is made up of a current mirror circuit. Such active load is used extensively in MOSFET circuits because a MOSFET transistor channel behaviour like a good active resistive load.
- The gain stage is made up of the common-source amplifier based on M6. This also has the current mirror M8, M9 as an active load.
- The output stage is a common-source output stage (also known as class A amplifier). M11 provides the bias to the circuit.

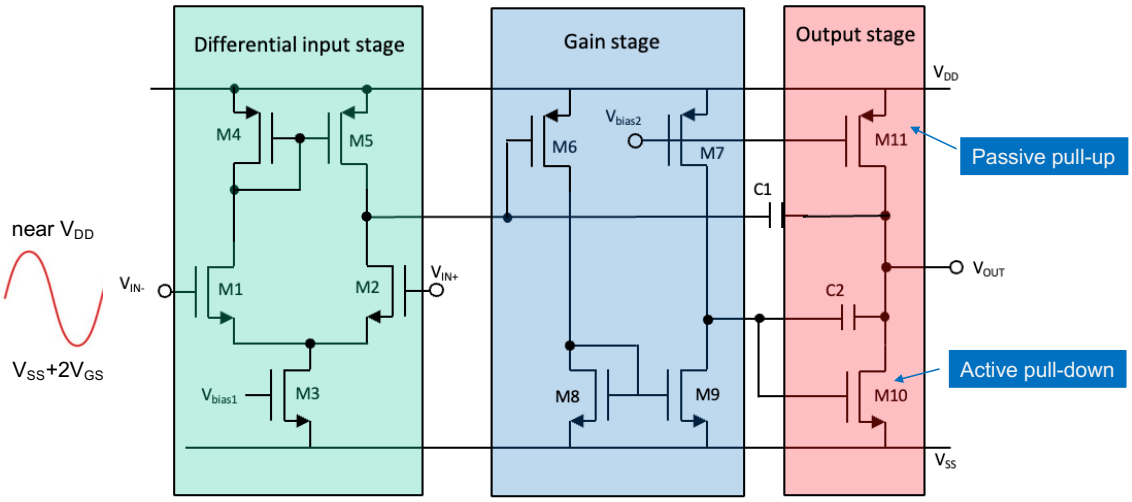
The use of MOSFET transistor as input allows the op-amp to have extremely high input impedance. For MCP6001, the op-amp used in Lab 1 experiment, the input impedance is around 10TΩ!

| **Input Bias Current and Impedance** | | | | | | |
|---|---|---|---|---|---|---|
| Input Bias Current: | $I_B$ | — | ±1.0 | — | pA | |
| Industrial Temperature | $I_B$ | — | 19 | — | pA | $T_A$ = +85°C |
| Extended Temperature | $I_B$ | — | 1100 | — | pA | $T_A$ = +125°C |
| Input Offset Current | $I_{OS}$ | — | ±1.0 | — | pA | |
| Common-Mode Input Impedance | $Z_{CM}$ | — | $10^{13}$\|\|6 | — | Ω\|\|pF | |
| Differential Input Impedance | $Z_{DIFF}$ | — | $10^{13}$\|\|3 | — | Ω\|\|pF | |

## n-type input MOSFETs but not rail-to-rail

- Similar op-amp is obtained by:
  - Flip circuit up-side-down.
  - Replace all n-type with p-type and vice versa.

- Not rail-to-rail input or output.
- Asymmetrical output drive.
- Bad for low-voltage, single supply.





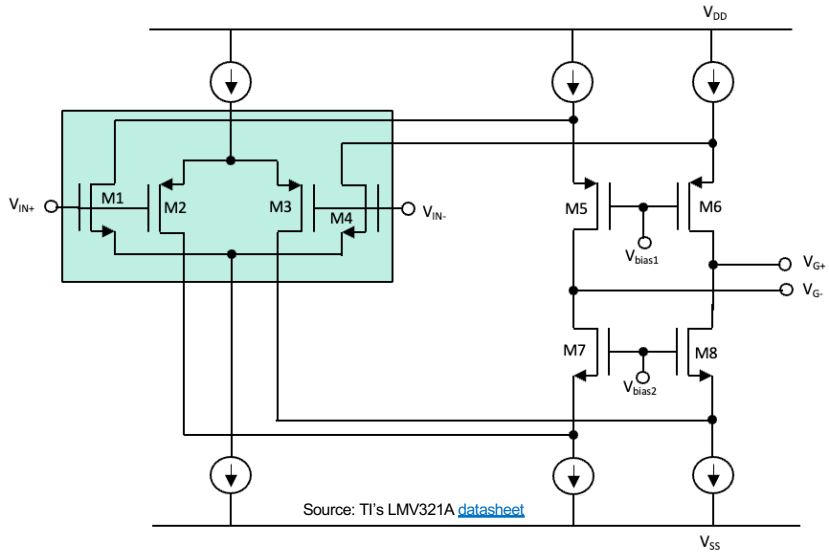

Interestingly, we can produce similar performing op-amp by swapping all p-type MOSFETs with n-type, and all n-type with with p-type as shown in the slide.

In both cases, there are two main problems:

1. n-type differential inputs as shown here can accept input voltages up to $V_{DD}$. However, the input stage will not remain linear unless the input signals are somewhat above Vss, (at around 2 x Vgs). Therefore this architecture will not accept rail-to-rail input signals.
2. The output stage is not suitable for driving an output load symmetrically either. It has active pull down (with M10), but M11 is effective a resistive load.

## Complementary differential input

- Use complementary differential input to solve input rail-to-rail issue.




Source: TI's LMV321A datasheet

| | | | | | | |
|---|---|---|---|---|---|---|
| Common-Mode Input Range | $V_{CMR}$ | $V_{SS} - 0.3$ | — | $V_{DD} + 0.3$ | V | Source: MCP6001 datasheet |



To solve the input voltage range problem, modern op-amps such as TI's LMV358 and Microchip's MC6001 uses a complementary differential input circuit as shown above. A pair of p-type differential circuit is connected in **parallel** with a pair of n-type differential circuit. The PMOS transistors allows input voltage to reach near $V_{SS}$, while the NMOS transistors support input voltage near $V_{DD}$.

This circuit configuration also provides added advantage that the circuit is now symmetrical, and provides 2nd stage complementary outputs to drive the output stage of the amplifier, as will be seen in the next slide.

The circuit diagram shown above is taken from TI's LMV321A datasheet, which can found here:

https://shorturl.at/JCYeu

We use MCP6001 rail-to-rail op-amp in the lab. Unfortunately, Microchip does not provide any internal circuit for their op-amp. Nevertheless, the technique described here is general practice among such op-amp designs. As seen from the MCP6001 datasheet (https://shorturl.at/CWGwl), the input voltage range can be within 300mV of the supply voltages.

## Op-amp Input Specifications

- These are the input specifications for the MCP6001 op-amp.

| | | | | | | |
|---|---|---|---|---|---|---|
| **Input Offset** | | | | | | |
| Input Offset Voltage | $V_{OS}$ | -4.5 | — | +4.5 | mV | $V_{CM} = V_{SS}$ **(Note 1)** |
| Input Offset Drift with Temperature | $\Delta V_{OS}/\Delta T_A$ | — | ±2.0 | — | µV/°C | $T_A$= -40°C to +125°C, $V_{CM} = V_{SS}$ |
| Power Supply Rejection Ratio | PSRR | — | 86 | — | dB | $V_{CM} = V_{SS}$ |
| **Input Bias Current and Impedance** | | | | | | |
| Input Bias Current: | $I_B$ | — | ±1.0 | — | pA | |
| Industrial Temperature | $I_B$ | — | 19 | — | pA | $T_A$ = +85°C |
| Input Offset Current | $I_{OS}$ | — | ±1.0 | — | pA | |
| Common-Mode Input Impedance | $Z_{CM}$ | — | $10^{13}$\|\|6 | — | Ω\|\|pF | |
| Differential Input Impedance | $Z_{DIFF}$ | — | $10^{13}$\|\|3 | — | Ω\|\|pF | |
| **Common-Mode** | | | | | | |
| Common-Mode Input Range | $V_{CMR}$ | $V_{SS}$ – 0.3 | — | $V_{DD}$ + 0.3 | V | |
| Common-Mode Rejection Ratio | CMRR | 60 | 76 | — | dB | $V_{CM}$ = -0.3V to 5.3V, $V_{DD}$ = 5V |

Highlighted entries are implemented in the MCP6001 LTSpice model.

Source: MCP6001 datasheet

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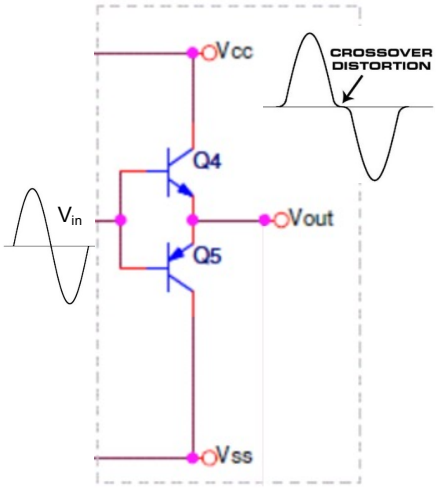
One of the learning outcomes of this lecture is to learn how to interpret an op-amp's datasheet.

Here are the various specification relating to the input stage of the MCP6001 op-amp.

1. **Input offset voltage** – when both V+ and V- inputs are connected to the same potential, any mismatch in the input transistors manifests this as an offset voltage between the two input terminals.
2. **Input offset drift** – this measures the change in input offset voltage with temperature.
3. **Power Supply Rejection Ratio (PSRR)** – this measures how much power supply noise get fed to the output. Since it is a rejection ratio, it is supply+noise(rms)/ output(rms) in dB. PSRR is a function of frequency (see datasheet graphs).
4. **Input bias current** – this is the quiescent current into the gate of each input MOSFET.
5. **Input offset current** – this measures the difference between the current flowing into V+ and V-.
6. **Common-mode input impedance** – this is the impedance measured between either input terminals and ground.
7. **Differential input impedance** – this is the impedance measured between the V+ and V- terminals.
8. **Common-mode input range** – this measures the range of voltages that can be applied to both V+ and V- at the same time.
9. **Common-mode rejection ration** (CMRR) – this measures how much common-mode signals get to the output. CMRR is a function of signal frequency (see datasheet graphs).

## Output Stage – Class B




- Yr 1st ADC part 2 Lecture 6, S3-5
- Q4 is emitter follower (Common-Emitter) for sourcing current to Vout (PUSH)
- Q5 is another emitter follower for sinking current from Vout (PULL)
- This is known as a PUSH-PULL or class B amplifer circuit
- $\delta Vout \approx \delta V_{in,}$ i.e. its gain is 1
- Each transistor only operate for half cycle or 180° of a sinewave signal
- Further, Q4 and Q5 requires VBE > 0.7V to start conducting, therefore this amplifier has distortion.



The output stage of BJT op-amps normally consists of complementary transistors Q4 and Q5. They each acts as an emitter follower circuit for the positive and negative half of $V_{IN}$ (as a sine wave) relative to the quiescent condition of $V_{out}$. This circuit structure is known as the "Push-Pull" configuration or a class AB amplifier.

If $V_{in} \geq V_{out}$(quiescent) + 0.7V, Q4 provides current to drive $V_{out}$ to $V_{in} - V_{BE4}$. This is known as "push" action - it sources current to the output load.

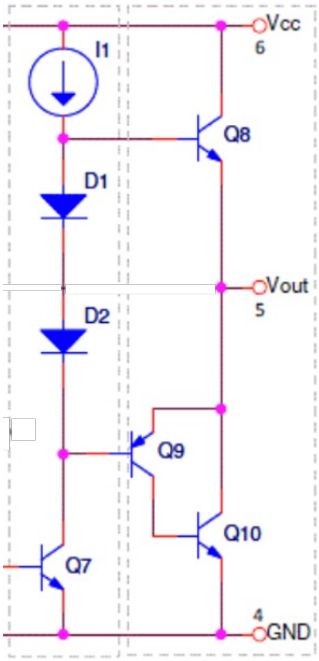
If $V_{in} \leq V_{out}$(quiescent) - 0.7V, Q5 absorbs current to drive $V_{out}$ to $V_{in} + V_{BE5}$. This is known as "pull" action - it sinks current from the output load.

This circuit incurs significant distortion when $-0.7 \leq V_{in} \leq +0.7$. During such crossover region, neither Q4 nor Q5 is conducting and the output is not effectively driven. Therefore, this amplifer always causes distortion at the crossover.

The small signal voltage gain of the 3rd stage is approximately 1.

This push-pull amplifier is also known as a class B amplifier. It is inherently more efficient than a class A (common emitter or common source) amplifer.

## Bipolar output Stage – Class AB output




- Q8 push emitter follower sourcing current
- Q9, Q10 pull emitter follower sinking current
- D1, D2 forward bias due to $I_1$
- Keep Q8 and Q9 in linear region – reduce distortion
- Q9 PNP has poor current gain
- Combine with Q10 NPN to boost current gain
- Q9, Q10 - called a "**Sziklai**" pair (different from Darlington pair)
- Av ≈ 1



Shown here is a common output stage in BJT op-amps.

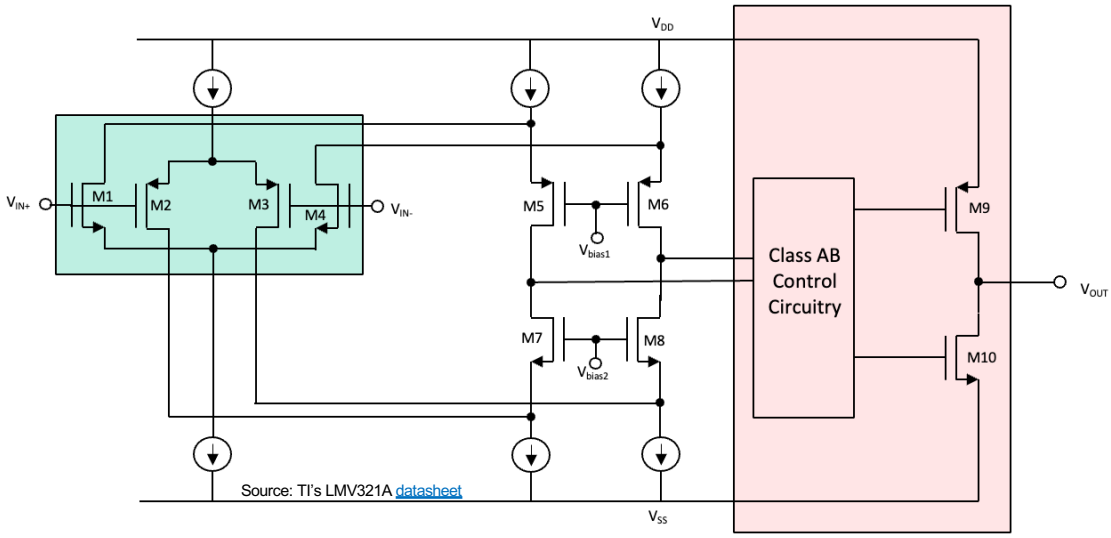
The simple push-pull circuit shown in the previous slide exhibits severe distortion because the NPN and PNP transistors are not conducting whenever their base-emitter voltages are below 0.7V. This is mitigated by adding two diodes D1 and D2 as shown. These two diodes are forward biased via the constant current source I1, and they ensure that both Q8 and Q9 are always operating in the linear region (i.e. base-emitter forward biased). This eliminates much of the distortion.

The second feature in the circuit above is that the PNP transistor is enhanced with Q10, a NPN transistor. The reason is that PNP transistors typically have significantly lower current gain than NPN transistors.

By adding Q10, the combined current gain is boosted to: $\beta \approx \beta_9 \beta_{10}$. This configuration is known as a "**Sziklai** transistor pair". It is different from **Darlington pair** which consists of two transistors of the SAME TYPE connected in cascade.

Sziklai transistor pair, like a Darlington pair, provides the same improved current gain (product of the two transistors' current gains), but it requires only one $V_{BE}$ to turn on, and not two, as in a standard Darlington configuration.

## Class AB output of MOSFET op-amp




- Improved output stage cannot drive low impedance load, say 8Ω speaker.

| | | | | | | |
|---|---|---|---|---|---|---|
| Output Short-Circuit Current | $I_{SC}$ | — | ±6 | — | mA | $V_{DD}$ = 1.8V |
| (Source: MCP6001 datasheet) | | — | ±23 | — | mA | $V_{DD}$ = 5.5V |



For MOSFET op-amp such as the MCP6001, the output stage also uses the push-pull arrangement. Since both output transistors always operates in the linear region (thanks to the control circuitry), this is also a class AB output.

In spite of having a better output stage with minimal cross-over distortion, such an output stage is unable to drive low impedance load such as an 8Ω speaker (as used in the lab). According to the datasheet of the MCP6001, the short-circuit current (the maximum possible output current) is limited to ±23mA with a 5.5V supply.

One could design an op-amp with output transistors that can handle much higher output current. Even so, such a design would be inefficient in terms of power dissipation. This is because all load current will flow through either M9 or M10, wasting energy.

For the lab experiment, you will be using a different type of amplifier to drive the low impedance speaker – the class D amplifier.

# Op-amp Output Specifications

- These are the output specifications for the MCP6001 op-amp.

| Output | | | | | | |
|---|---|---|---|---|---|---|
| Maximum Output Voltage Swing | $V_{OL}$, $V_{OH}$ | $V_{SS}$ + 25 | — | $V_{DD}$ – 25 | mV | $V_{DD}$ = 5.5V, 0.5V input overdrive |
| Output Short-Circuit Current | $I_{SC}$ | — | ±6 | — | mA | $V_{DD}$ = 1.8V |
| | | — | ±23 | — | mA | $V_{DD}$ = 5.5V |

Highlighted entries are implemented in the MCP6001 LTSpice model.

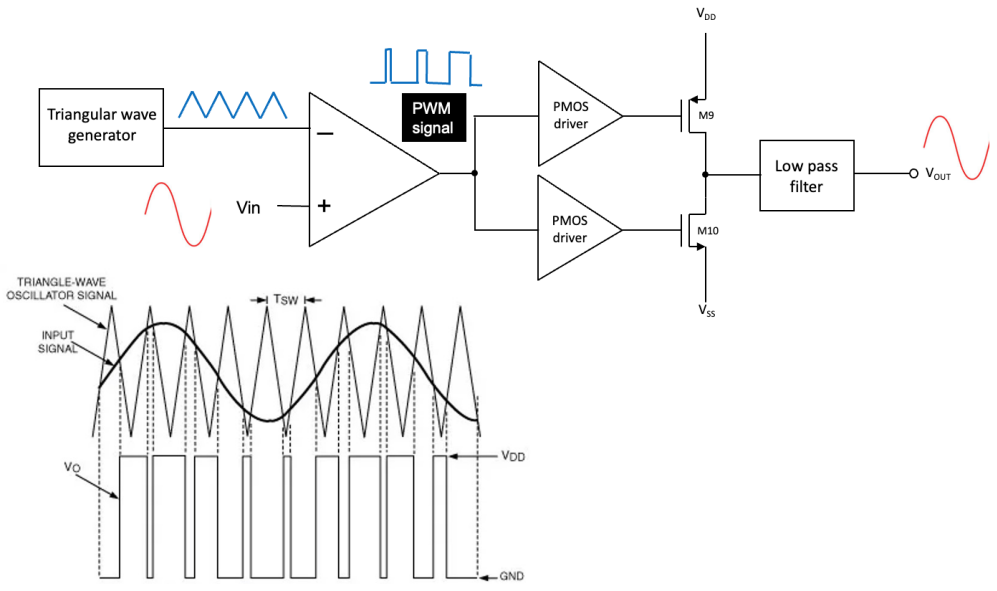
Source: MCP6001 datasheet



Here are the various specification relating to the output stage of the MCP6001 op-amp.

1. **Maximum output voltage swing** – this is the range of voltages that the output can drive a load. For this rail-to-rail op-amp with Class AB output, the output can swing to within 25mV of the supply voltages.
2. **Output Short-Circuit Current** – this is the maximum current that can be supplied or sunk by the output stage of the op-amp. This is not the same as the output impedance of the op-amp, but is related to it indirectly because the op-amp output impedance is NOT linear.

# Block Diagram of a Class D amplifier






This block diagram shows the structure of a typical class D amplifier.

In a class D amplifier, the input signal is first converted to a pulse-width modulated signal (PWM), where the width of a continuous period pulse sequence is proportional to the signal amplitude. This is shown in the waveform above.

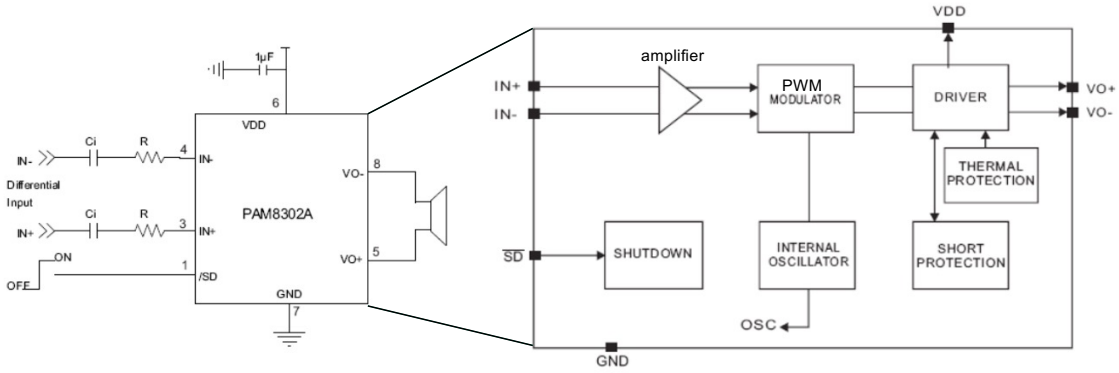
A PWM circuit consists of a triangular wave generator and a comparator. You will be building a PWM circuit in Lab 2 as one of the tasks.

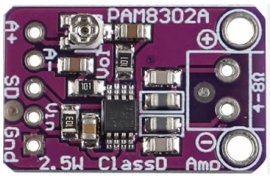
The output from the PWM circuit, through driver circuits, is used to drive the push-up PMOS and the pull-down NMOS output transistor which can handle high current.

The output signal is then passed through a lowpass filter to remove the high frequency components produced through the pulse-width modulation process.

The reason why a class D amplifier is far more efficient than class A, B or AB amplifier is that the PMOS and NMOS output transistors are either ON or OFF, and never operate in the linear region. When it is ON, the current through the transistor is high, but the voltage drop across the drain and source is small, and vice versa.

# The PAM8302A Audio Amplifier




- 2.5W Output at 10% THD with a 4Ω Load and 5V Power Supply
- Filterless, Low Quiescent Current and Low EMI
- High Efficiency up to 88%
- Superior Low Noise
- Short Circuit Protection

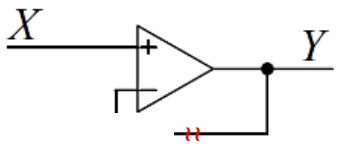


The class D amplifier we use in the Lab to drive the 8Ω speaker is PAM8302A. Shown here is the functional block diagram of this amplifier. It is capable of a load as low as 8Ω and has a power efficiency of up to 88%.

You do not need to understand the inner working of this amplifier, but the datasheet is available to download via the course webpage.

## Stability issue in op-amps

- Op-amp as an amplifier always uses NEGATIVE FEEDBACK to determine the gain.
- Consider this unity gain buffer: break the loop in the feedback path.
- Due to delay, could feedback a signal that is 180º out of phase relative to input.
- The negative feedback now become positive feedback, leading to oscillation.




Gain = 1

**Stability requirement:**

1. The open-loop **gain is > 1**, but the **phase angle** must be **<180º** at **all signal frequencies**, OR
2. The **phase angle** is **≥ 180º**, but the open-loop **gain is < 1** at **all signal frequencies**.



All op-amp are designed to have high DC gain. Feeding back all or part of the output signal to the negative input in op-amp circuits allow us to fix the gain of the amplifier using ONLY resistor ratio. This however create a potential problem in instability, which may result in oscillation at the output.

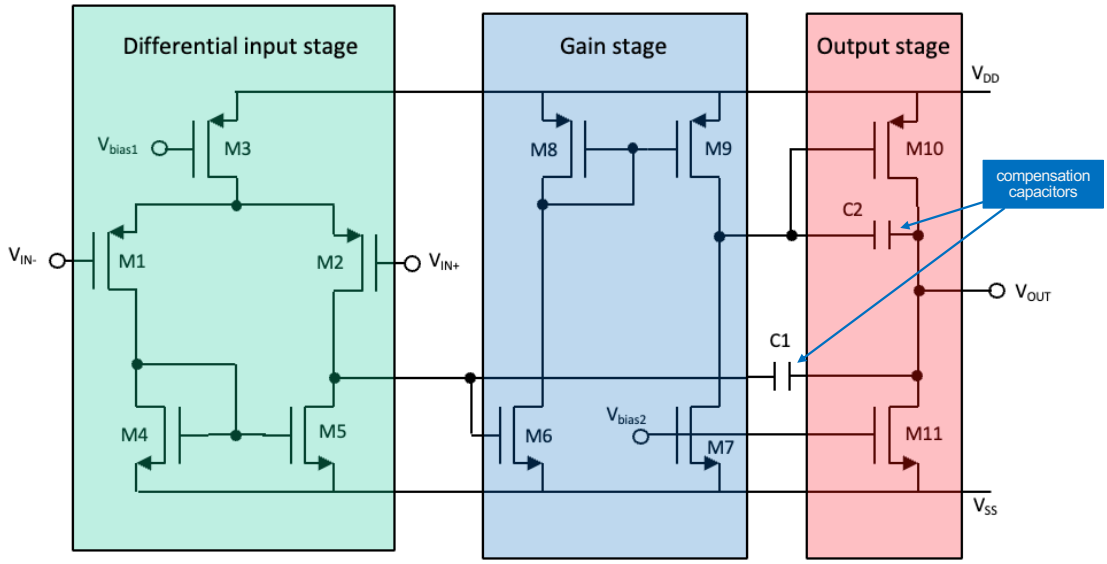
The cause of such problem is due to the **delay** that is introduced as a signal moves from input to output. Such delay in general increases as signal frequency increases.

If the delay causes a signal to exhibit a phase shift of 180º, then the feedback signal will changes the sign (180º phase shift = multiply by -1). Negative feedback becomes positive feedback. If the loop gain of the op-amp circuit is greater than 1, then the feedback signal will result in output going higher at that frequency resulting in indefinite oscillation.

This could happen at any frequency, because if this situation is possible, the op-amp circuit will latch onto such oscillation frequency from any external disturbance (e.g. power on transient).

Therefore, to ensure an op-amp does not go into oscillation when feedback is used in any application, either the loop gain must be lower than 1 or the phase shift introduced must be below 180º at all frequencies.

# Open-loop gain and compensation capacitors






To satisfy the stability requirement in op-amps, designers insert a compensation capacitor C1 into the op-amp circuit. This effectively introduce a pole (like a RC circuit) at relatively low frequency (typically 2Hz to 20Hz).

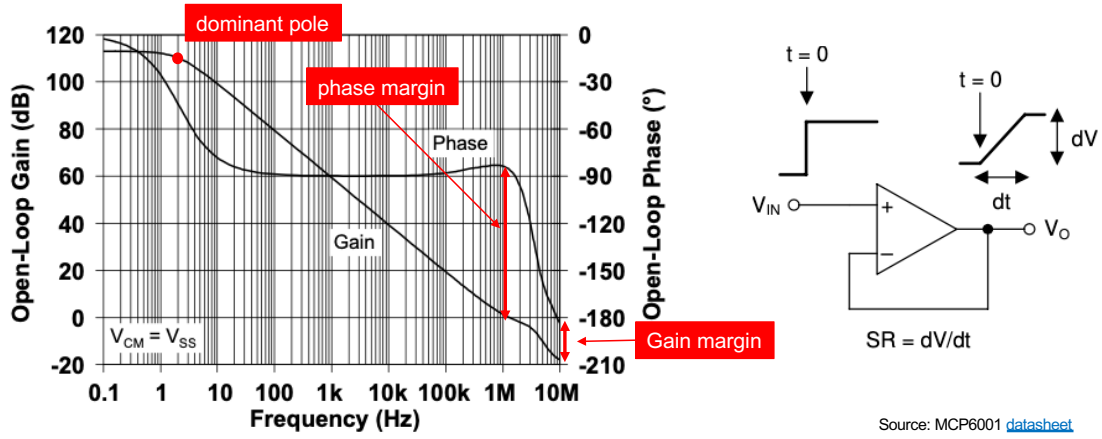
This introduces a 20dB/decade drop in open-loop gain to the amplifier. In this way, when the amplifier exhibits 180 degree phase shift at a high frequency, the gain of the amplifier is drop to below 1 (or 0dB). The risk of oscillation is therefore averted.

In some op-amps, a second compensation capacitor C2 may be introduced to future reduce the gain at some higher frequency.

# Op-amp Loop Gain specification

| Open-Loop Gain | | | | | | |
|---|---|---|---|---|---|---|
| DC Open-Loop Gain (Large Signal) | $A_{OL}$ | 88 | 112 | — | dB | $V_{OUT}$ = 0.3V to $V_{DD}$ – 0.3V, $V_{CM}$ = $V_{SS}$ |

| AC Response | | | | | | |
|---|---|---|---|---|---|---|
| Gain Bandwidth Product | GBWP | — | 1.0 | — | MHz | |
| Phase Margin | PM | — | 90 | — | ° | G = +1 V/V |
| Slew Rate | SR | — | 0.6 | — | V/µs | |




Source: MCP6001 datasheet



The MCP6001 has a compensation capacitor that introduces a dominant pole at 2Hz. The DC open-loop gain is 112dB, or ~400,000.

The gain is reduced at a rate of -20dB/decade (i.e. gain drop by a factor of 10 for as frequency increases by a factor of 10). The gain of the op-amp drops to 0dB (i.e. x1 gain) at 1MHz. This is known as the Gain-Bandwidth Product (GBP). At 1MHz, the phase shift introduced by this op-amp is only around -90º. Hence there is no chance of this op-amp becoming unstable under any feedback condition.

Finally, slew rate limit (SR) measures how fastest rate at which the output can change as input changes suddenly. For the MCP6001, SR is only 0.6V/us. Note that the slew rate is related to the dominant pole frequency introduced by the compensation capacitor. The result of the limit in the slew rate is because there is maximum current available internally to charge the compensation capacitor(s). Given a fixed maximum current, the value of C determines both the break frequency (i.e. 2Hz) and the slew rate.

So far, we have ignored the noise specification because we are not using this in our lab experiment and we also do not model this in the LTSpice model later.